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Г	APPLICATION NO.	FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
	10/811,189	03/26/2004		Bruce A. Hecht	A0312.70490US01	2956
	7:	590	12/20/2005		EXAMINER	
	William R. M Wolf, Greenfie			TAN, VIBOL		
	600 Atlantic Avenue				ART UNIT	PAPER NUMBER
	Boston, MA	02210			2819	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)					
		10/811,189	HECHT ET AL.					
	Office Action Summary	Examiner	Art Unit					
		Vibol Tan	2819					
Period fo	The MAILING DATE of this communication ap r Reply	pears on the cover sheet with t	he correspondence address					
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Status								
1) 🏻	Responsive to communication(s) filed on <u>01 E</u>	December 2005						
· ·		s action is non-final.						
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-/	closed in accordance with the practice under	•	•					
Dispositi	on of Claims							
4)⊠	Claim(s) <u>1,2,6-8,10-13,15-20,24-26 and 28</u> is/							
•	4a) Of the above claim(s) is/are withdra							
	Claim(s) is/are allowed.							
	Claim(s) <u>1,2,6-8,10-13,15-17,19,20 and 28</u> is/	are rejected.						
	Claim(s) 18 and 24-26 is/are objected to.	•						
· · · —	Claim(s) are subject to restriction and/o	or election requirement.						
Applicati	on Papers	•						
9)□ .	The specification is objected to by the Examine	er.						
-	The drawing(s) filed on is/are: a) ☐ acc		he Examiner.					
•	Applicant may not request that any objection to the	•						
	Replacement drawing sheet(s) including the correct	= * *	• •					
	The oath or declaration is objected to by the Ex		• • • • • • • • • • • • • • • • • • • •					
Priority u	nder 35 U.S.C. § 119							
_	Acknowledgment is made of a claim for foreign ☐ All b)☐ Some * c)☐ None of:	priority under 35 U.S.C. § 11	9(a)-(d) or (f).					
a)ر	1. ☐ Certified copies of the priority document	e have been received						
	2. Certified copies of the priority document		cation No					
	3. Copies of the certified copies of the prior							
	application from the International Burea	•	orved in this reasonal stage					
* S	ee the attached detailed Office action for a list	, , , , , , , , , , , , , , , , , , , ,	eived.					
Attachment	(s)							
	e of References Cited (PTO-892)	4) 🔲 Interview Sumn						
	e of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Ma						
	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) No(s)/Mail Date	6) Other:	nal Patent Application (PTO-152)					

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 1, 2, 6-8, 11, 12, 16 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Hecht et al. (U.S. Pat. 6,507,231).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Hecht et al. teaches in Figs. 2 & 3, a method for operating a driver circuit, comprising: operating the driver circuit (20) at full power in a dynamic mode (when transmitting); and operating the driver circuit at reduced power in a termination mode (not transmitting), wherein operating the driver circuit at reduced power comprises reducing a slew current (29) for an output stage (24) of the driver circuit, further comprising maintaining Application/Control Number: 10/811,189

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an idle current (27) for the output stage at a constant level in the dynamic mode and in the termination mode.

In claim 2, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit at reduced power comprises reducing or turning off at least one current (all other switching transistors are off; col. 5, line 50) in the driver circuit in the termination mode.

In claim 6, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit (20) at reduced power further comprises reducing bias current (a current used to bias x1) to a reverse buffer (x1) of the driver circuit.

In claim 7, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit at reduced power further comprises reducing bias current (gate current) to a digital input circuit (Q29, Q75) of the driver circuit.

In claim 8, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit at reduced power further comprises reducing bias current to input buffers (30A, 30B) that supply programmable levels to an output stage (24) of the driver circuit.

In claim 11, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit at full power comprises selectably operating in a high state (logic 1), a low state (logic 0) or an inhibit state (high impedance) in the dynamic mode (transmitting mode).

In claim 12, Hecht et al. further teaches, the method as defined in claim 1, wherein operating the driver circuit at a reduced power comprises selectably operating in a high

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state (logic 1), a low state (logic 0) or an inhibit state (high impedance) in the termination mode (not transmitting).

Claim 16 corresponds to detailed circuitry already discussed similarly with regard to method claim 1.

Claim 28 corresponds to detailed circuitry already discussed similarly with regard to method claim 1.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 10, 13, 15, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hecht et al. in view of Kardash (U.S. Pat. 6,137,329).

In claim 10, Hecht et al. teaches all the claim features the method of claim 1; with the exception of teaching wherein operating the driver circuit at reduced power comprises reducing at least one bias current to the driver circuit using a current multiplier. However, Kardash teaches in Fig. 2 a current multiplier 60 is used in a controller for controlling the voltage slew-rate of a load.

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention was made to incorporate a current multiplier, as taught by Kardash, into the device of Hecht et al. in order to control the reduction of current flow; thus reducing power.

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Claim 13 corresponds to detailed circuitry already discussed similarly with regard to method claim 10.

In claim 15, Hecht et al. further teaches, the driver circuit as defined in claim 13, wherein the mode control circuit is configured to reduce at least one current (all other switching transistors are off; col. 5, line 50) in the driver circuit in the termination mode.

Claim 17 corresponds to detailed circuitry already discussed similarly with regard to method claim 10.

In claim 19, Kardash further teaches the driver circuit as defined in claim 17, wherein an output current of the current multiplier is about 2 to 30 times (K= 10; col. 4, line 13) the control current.

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hecht et al. in view of Kardash and further in view of Lau et al. (U.S. Pat. 5,146,159).

In claim 20, Hecht et al. in view of Kardash teaches all claimed feature of the diver circuit of claim 16; with the exception of teaching wherein the output circuit comprises a class AB output circuit. However, Lau et al. teaches in claim 10, the pin driver in which the predriver stage is a forward biased for class AB operation for maintaining a low quiescent current of the test signal.

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hecht et al. and the teachings of Kardash and further the teachings of Lau et al. in order to maintain a low quiescent current of the test signal.

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6. Claims 18 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 13, 16 and 28 have been considered but are most in view of the new ground(s) of rejection.

The newly applied reference of Hecht et al. anticipates claims 1, 2, 6-8, 11, 12, 16 and 28 under 35 U.S.C. 102(e) with a common inventor, as set forth above.

The reference of Hecht et al. in combination with Kardash teaches the claimed limitations of claims 10, 13, 15, 17 and 19.

Finally, Hecht et al. in view of Kardash and further in view of Lau teaches claimed features of claim 20.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER